REMARKS/ARGUMENTS

Claims 21-32 were previously pending in the application. Claims 24, 28, and 32 are canceled, and claims 21, 25, and 29 are amended herein. Assuming the entry of this amendment, claims 21-23, 25-27, and 29-31 are now pending in the application. The Applicant hereby requests further examination and reconsideration of the application in view of the foregoing amendments and these remarks.

In paragraph 2 of the final office action, the Examiner rejected claims 21-32 under 35 U.S.C. 102(e) as being anticipated by Maiyuran. For the following reasons, the Applicant submits that the pending claims are allowable over Maiyuran.

This Amendment Does Not Raise Any New Issues

Claim 21 has been amended to include the features of previously pending claim 24. As such, currently amended claim 21 is equivalent to previously pending claim 24 rewritten in independent form. Similarly, claims 25 and 29 have been amended to include the features of previously pending claims 28 and 32, respectively. As such, currently amended claims 25 and 29 are equivalent to previously pending claims 28 and 32, respectively, rewritten in independent form. The Applicant submits therefore that the current amendment does not raise any new issues that would prevent the Examiner from considering this amendment.

Maiyuran Does Not Teach All of the features of Currently Amended Claims 21, 25, and 29

According to currently amended claim 21, the apparatus comprises first, second, and third circuitry. The first circuitry (1) receives a fetch address, (2) determines a set associated with the fetch address, (3) reads *Y* address tags and *Y* states corresponding to the associated set, (4) determines which of the *Y* address tags are valid based on the *Y* states, (5) compares the fetch address to one or more valid address tags, and (6) generates, if one of the valid address tags matches the fetch address, a first control signal indicating that the block associated with the matching valid address tag is a matching block. In particular, the first circuitry comprises a first latch that latches the fetch address.

The second circuitry (1) receives the fetch address, (2) receives the first control signal generated by the first circuitry, (3) generates a second control signal based on the first control signal and indicating the matching block, (4) generates block-enable control signals for the cache memory, (5) applies the block-enable control signals to the cache memory, such that the matching block in the cache memory is enabled and the (*Y*-1) other blocks in the cache memory are at least partly disabled, and (6) applies the fetch address to the cache memory to read one or more associated words from the enabled matching block. In particular, the second circuitry comprises (i) a second latch that latches the first control signal and outputs the second control signal and (ii) a plurality of other latches that latch the block-enable control signals.

The third circuitry is connected to an output of each block of the cache memory and (1) receives the second control signal generated by the second circuitry, (2) receives the one or more associated words from the enabled matching block, and (3) selects the one or more associated words for output from the cache memory based on the second control signal. In particular, the third circuitry comprises a multiplexer that receives the outputs from the blocks and selects the one or more associated words from the enabled matching block based on the second control signal from the second latch.

In rejecting previously pending claim 24, in paragraph 6, the Examiner cited column 9, lines 38-45, of Maiyuran as teaching "a first latch adapted to latch the fetch address." Significantly, the

disclosure at column 9, lines 38-45, is related to prior-art FIG. 5, which illustrates "cache organization according to conventional techniques" (see column 9, lines 33-34), which do not partly disable any blocks in the cache memory, while one or more blocks are enabled. See, e.g., column 1, lines 36-39 ("It is known to disable (e.g., power down) a processor cache when it is not in use in order to save power. Such a technique, however, disables the cache entirely and can be used only when the cache has no operation to perform.") As such, the latches referred to in column 9, lines 38-45, are not part of Maiyuran's invention.

Furthermore, latches 730-760 described in column 9, lines 38-45, store addressed data. See, e.g., column 9, lines 43-44 ("Addressed data may propagate from the banks to a set of latches 730-760.") According to claim 24, the first latch in the first circuitry latches "the fetch address." A fetch address is simply not addressed data. As such, none of latches 730-760 can be said to be an example of the first latch of currently amended claim 21.

Similarly, the Examiner cited column 9, lines 38-45, of Maiyuran as teaching "a second latch adapted to latch the first control signal and output the second control signal." Note that the first control signal, which is generated by the first circuitry of claim 21, indicates whether the block associated with a matching valid address tag is a matching block.

Here, too, latches 730-760 described in column 9, lines 38-45, are not part of Maiyuran's invention. Here, too, latches 730-760 store addressed data. Maiyuran's addressed data is simply not an example of a control signal that indicates whether a block associated with a matching valid address tag is a matching block. As such, none of latches 730-760 can be said to be an example of the second latch of currently amended claim 21.

Claim 24 recited (and now claim 21 recites) that the second circuitry comprises a plurality of other latches adapted to latch the block-enable control signals. Significantly, in rejecting claim 24, the Examiner completely ignored this explicitly recited feature of the claim. The Applicant submits that Maiyuran does not teach any latches that are analogous to "the plurality of other latches" explicitly recited in claim 21.

In addition, the Examiner cited column 10, lines 9-30, as teaching the multiplexer of claim 24. According to claim 24 (and now claim 21), the multiplexer receives the outputs from the blocks and selects the one or more associated words from the enabled matching block based on the second control signal from the second latch. Column 10, lines 9-30, does not describe a multiplexer that receives outputs from block and selects one or more associated words form an enabled matching block based on a second control signal from a second latch. As such, column 10, lines 9-30, cannot be said to teach an example of the multiplexer of claim 21.

In order to be anticipated under 35 U.S.C. 102(e), all of the elements of Applicant's invention as claimed must be present in the allegedly anticipating reference. Since Maiyuran does not disclose each and every element of previously presented claim 24, the rejection of claim 24 under Maiyuran was improper. Since currently amended claim 21 is equivalent to previously presented claim 24 rewritten in independent form, the Applicant submits that currently amended claim 21 is allowable over Maiyuran.

For similar reasons, the Applicant submits that currently amended claims 25 and 29 are also allowable over Maiyuran. Since claims 22-23 depend from claims 21, claims 26-27 depend from claim 25, and claims 30-31 depend from claim 29, it is further submitted that those claims are also allowable over Maiyuran.

In view of the above amendments and remarks, the Applicant believes that the now-pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

Date: October 9, 2007
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